Statement of Volatility – Dell PowerEdge R630

The Dell PowerEdge R630 contain both volatile and non-volatile (NV) components. Volatile components lose their data immediately upon removal of power from the component. Non-volatile components continue to retain their data even after the power has been removed from the component. Components chosen as user-definable configuration options (those not soldered to the motherboard) are not included in the Statement of Volatility. Configuration option information (pertinent to options such as microprocessors, remote access controllers, and storage controllers) is available by component separately. The following NV components are present in the PowerEdge R630 servers.

Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size
Planer				
PCH Internal CMOS RAM	Non-Volatile	1	U_PCH	256 Bytes
BIOS Password	Non-Volatile	1	U_PCH	16 bytes
BIOS SPI Flash	Non-Volatile	1	U_SPI_BIOS	8 MB
iDRAC SPI Flash	Non-Volatile	1	U_IDRAC_SPI	4 MB
BMC EMMC	Non-Volatile	1	U_EMMC	4 GB
CPU Vcore Regulators	Non-Volatile	2	U8003, U8043	512 Bytes
Vmem Regulators	Non-Volatile	2	U8011, U8051	512 Bytes
System CPLD RAM	Volatile	1	U_CPLD	1 KB

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Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size
System Memory	Volatile	Up to 12 per CPU	CPU<2:1>_CH<3:0>_D<2:0>	Up to 32GB per DIMM
Internal USB Key	Non-Volatile	Up to 1	N/A	Varies (not factory installed)
Trusted Platform Module (TPM)	Non-Volatile	1	U_TPM	128 Bytes
CPU	Volatile	1 or 2	CPU1 / CPU2	Various
iDRAC DDR	Volatile	1	U_IDRAC_MEM	256MByte
iDRAC	Volatile	1	U_IDRAC	64 kbyte + registers
8x2.5" Backplane				
SEP internal flash	Non-Volatile	1	U3	Flash:32KB+4KB EEPROM: 1KB
10x2.5" (or 6x2.5" + 4x PCIe SSD) EXP/Backplane				
NVSRAM memory	Non-Volatile	1	U1	1 Mb
Flash memory	Non-Volatile	1	U2	32 Mb
Expander FRU image	Non-Volatile	1	U5	512 Bytes
BP FRU image	Non-Volatile	1	U15	256 Bytes
24x2.5" EXP/Backplane				
NVSRAM memory	Non-Volatile	1	U3	1 Mb
Flash memory	Non-Volatile	1	U2	32 Mb
Expander FRU image	Non-Volatile	1	U7	512 Bytes
BP FRU image	Non-Volatile	1	U3	256 Bytes
H730, H830 PERCs				

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Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size
NVSRAM	Non-volatile	1	U1033	128KB
FRU	Non-volatile	1	U1019	256B
1-Wire EEPROM	Non-volatile	1	U1004	128B
SPD	Non-volatile	1	U22	256B
SBR	Non-volatile	1	U1020	8KB
Flash	Non-volatile	1	U1031	16MB
ONFI Backup Flash	Non-volatile	1	U1059	4GB
SDRAM	Volatile	5	U1043-U1047	512MB/1GB
H330, H330M PERC				
NVSRAM	Non-volatile	1	U1033	128KB
FRU	Non-volatile	1	U1019	256B
1-Wire EEPROM	Non-volatile	1	U1004	128B
SBR	Non-volatile	1	U1020	8KB
Flash	Non-volatile	1	U3	16MB
PCIe SSD Extension Card				
Switch Configuration EEPROM	Non-Volatile	1	U2	256B

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Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size
IDSDM				
SPI Flash	Non-Volatile	1	U2	8Mb
MCU	Non-Volatile	1	U6	512KB
x8 Control Panel				
rSPI Flash	Non-Volatile	1	U3	32Mb
x10/x24 Control Panel				
rSPI Flash	Non-Volatile	1	U6	32Mb
iDRAC Quick Sync				
MCU MSP430	Non-Volatile	1	U_MSP430	128KB

Item	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)
Planer			
PCH Internal CMOS RAM	Battery-backed CMOS RAM	No	Real-time clock and BIOS configuration settings
BIOS Password	Battery-backed CMOS RAM	Yes	Password to change BIOS settings
BIOS SPI Flash	SPI Flash	No	Boot code, system configuration information, UEFI environment, Flash descriptor, ME

Item	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)
iDRAC SPI Flash	SPI Flash	No	iDRAC Uboot (bootloader), server management persistent store (i.e. IDRAC MAC Address, iDRAC boot variables), lifecycle log cache, virtual planar FRU and EPPID, rac log, system event log, JobStore, iDRAC Secure boot code,
BMC EMMC	eMMC NAND Flash	No	Operational iDRAC FW, Lifecycle Controller (LC) USC partition, LC service diags, LC OS drivers, USC firmware
CPU Vcore Regulators	ROM	No	Operational parameters
Vmem Regulators	ROM	No	Operational parameters
System CPLD RAM	RAM	No	Not utilized
System Memory	DRAM	Yes	System OS RAM
Internal USB Key	Flash	Yes	General purpose USB key drive
Trusted Platform Module (TPM)	EEPROM	Yes	Storage of encryption keys
CPU	Cache + registers	Yes	Processor cache + registers
iDRAC DDR	DRAM	No	iDRAC local memory
iDRAC	Cache + registers	No	Processor cache + registers
8x2.5" Backplane			
SEP internal flash	Integrated Flash+EEPROM	No	Firmware + FRU
10x2.5" (or 6x2.5" + 4x PCIe SSD) EXP/Backplane			
NVSRAM memory	Flash	No	FW configuration data
Flash memory	Flash	No	Firmware

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Item	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)
Expander FRU image	I2C EEPROM	No	FRU
BP FRU image	I2C EEPROM	No	FRU
24x2.5" EXP/Backplane			
NVSRAM memory	Flash	No	FW configuration data
Flash memory	Flash	No	Firmware
Expander FRU image	I2C EEPROM	No	FRU
BP FRU image	I2C EEPROM	No	FRU
H730, H830 PERCs			
NVSRAM	NVSRAM	No	Configuration data
FRU	FRU	No	Card manufacturing information
1-Wire EEPROM	1-Wire EEPROM	No	Holds default controller properties/settings
SPD	SPD	No	Memory configuration data
SBR	SBR	No	Bootloader
Flash	Flash	No	Card firmware
ONFI Backup Flash	ONFI Backup Flash	No	Holds cache data during power loss
SDRAM	SDRAM	No	Cache for HDD I/O
H330, H330M PERC			
NVSRAM	NVSRAM	No	Configuration data
FRU	FRU	No	Card manufacturing information
1-Wire EEPROM	1-Wire EEPROM	No	Holds default controller

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Item	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)
			properties/settings
SBR	SBR	No	Bootloader
Flash	Flash	No	Card firmware
PCIe SSD Extension Card			
Switch Configuration EEPROM	SPI Flash EEPROM	No (requires specialized SW)	Configuration for PLX PCIe switch, setting registers
IDSDM			
SPI Flash	SPI Flash	No	Exclusively used by the controller
MCU	Embedded Flash	FW can be updated via iDRAC which runs on Linux	Firmware
x8 Control Panel			
rSPI Flash	SPI Flash	No	restored SPI
x10/x24 Control Panel			
rSPI Flash	SPI Flash	No	restored SPI
iDRAC Quick Sync			
MCU MSP430	Flash	No	iDRAC Quick Sync Communicate Protocol

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Item	How is data input to this memory?	How is this memory write protected?	How is the memory cleared?
Planer			
PCH Internal CMOS RAM	BIOS	N/A – BIOS only control	1) Set NVRAM_CLR jumper to clear BIOS configuration settings at boot and reboot system; 2) AC power off system, remove coin cell battery for 30 seconds, replace battery and power back on; 3) restore default configuration in F2 system setup menu.
BIOS Password	Keyboard	N/A	Place shunt on J_PSWD_NVRAM jumper pins 2 and 4.
BIOS SPI Flash	SPI interface via iDRAC	Software write protected	Not possible with any utilities or applications and system is not functional if corrupted/removed.
iDRAC SPI Flash	SPI interface via iDRAC	Embedded iDRAC subsystem firmware actively controls sub area based write protection as needed.	Not completely user clearable; however, user data, lifecycle log and archive, SEL, fw image repository can be cleared via Delete Configuration and Retire System, accessible in Lifecycle Controller interface
BMC EMMC	NAND Flash interface via iDRAC	Embedded FW write protected	Not completely user clearable; however, user data, lifecycle log and archive, SEL, fw image repository can be cleared via Delete Configuration and Retire System, accessible in Lifecycle Controller interface
CPU Vcore Regulators		NA	Not user clearable
Vmem Regulators		NA	Not user clearable
System CPLD RAM	Not utilized	Not accessible	Not accessible
System Memory	System OS	OS Control	Reboot or power down system
Internal USB Key	USB interface via PCH. Accessed via system OS	No write protect	Can be cleared in system OS
Trusted Platform Module (TPM)	Using TPM Enabled operating systems	SW write protected	F2 Setup option

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Item	How is data input to this memory?	How is this memory write protected?	How is the memory cleared?
CPU	Various	Various	Power off
iDRAC DDR	iDRAC Firmware	NA	Power off
iDRAC	iDRAC Firmware	NA	Power off
8x2.5" Backplane			
SEP internal flash	I2C interface via iDRAC	Program write protect bit	Not user clearable
10x2.5" (or 6x2.5" + 4x PCIe SSD) EXP/Backplane			
NVSRAM memory	Common Flash memory Interface (CFI)	Hardware strapping	Not user clearable
Flash memory	Common Flash memory Interface (CFI)	Hardware strapping	Not user clearable
Expander FRU image	I2C interface via iDRAC	Hardware strapping	Not user clearable
BP FRU image	I2C interface via iDRAC	Hardware strapping	Not user clearable
24x2.5" EXP/Backplane			
NVSRAM memory	Common Flash memory Interface (CFI)	Hardware strapping	Not user clearable
Flash memory	Common Flash memory Interface (CFI)	Hardware strapping	Not user clearable
Expander FRU image	I2C interface via iDRAC	Hardware strapping	Not user clearable
BP FRU image	I2C interface via iDRAC	Hardware strapping	Not user clearable
H730, H830 PERCs			
NVSRAM	ROC writes configuration data to NVSRAM	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
FRU	Programmed at ICT during production.	Not WP	Cannot be cleared with existing tools available to the customer
1-Wire EEPROM	ROC writes data to this memory	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
SPD	Pre-programmed before assembly	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer

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Item	How is data input to this memory?	How is this memory write protected?	How is the memory cleared?
SBR	Pre-programmed before assembly	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
Flash	Pre-programmed before assembly. Can be updated using Dell/LSI tools	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
ONFI Backup Flash	FPGA backs up DDR data to this device in case of a power failure	Not WP. Not visible to Host Processor	Flash can be cleared by powering up the card and allowing the controller to flush the contents to VDs. If the VDs are no longer available, cache can be cleared by going into controller bios and selecting Discard Preserved Cache.
SDRAM	ROC writes to this memory - using it as cache for data IO to HDDs	Not WP. Not visible to Host Processor	Cache can be cleared by powering off the card
H330, H330M PERC			
NVSRAM	ROC writes configuration data to NVSRAM	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
FRU	Programmed at ICT during production	Not WP	Cannot be cleared with existing tools available to the customer
1-Wire EEPROM	ROC writes data to this memory	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
SBR	Pre-programmed before assembly	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
Flash	Pre-programmed before assembly. Can be updated using Dell/LSI tools	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
PCIe SSD Extension Card			
Switch Configuration EEPROM	The EEPROM image is pre-loaded at factory before assembly. Once assembled on the card, data can be entered	Device can be write protected via hardware pin. Alternatively, device contents can be write protected via	System is not functional as intended if corrupted/removed.

Item	How is data input to this memory?	How is this memory write protected?	How is the memory cleared?
	via PLX Device Editor or PLX EEP DOS based tool.	WPEN bit in status register.	
IDSDM			
SPI Flash	SPI interface via iDRAC	Hardware strapping	Not user clearable
MCU	USB3.0 interface via PCH	N/A	Not user clearable
x8 Control Panel			
rSPI Flash	SPI interface via iDRAC	Hardware strapping	Not user clearable
x10/x24 Control Panel			
rSPI Flash	SPI interface via iDRAC	Hardware strapping	Not user clearable
iDRAC Quick Sync			
MCU MSP430	I2C interface via iDRAC	Hardware strapping	Not user clearable - It also auto-clears when power is applied.

NOTE: For any information that you may need, direct your questions to your Dell Marketing contact.

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